



(19) Japan Patent Office (JP)
(12) Laid-Open Patent Report (A)
(11) Laid-open patent application no.
S58-181310
(43) Date laid open: October 24, 1983

(51) Int. Cl.³:
H 03 G 3/02

Identification code: Internal control no.:
7154-5J
Number of inventions: 1
Inspection requested: Yes
(Total 3 pages)

(54) Title of the invention: Voltage gain control amplifier
(21) Application no.: S57-64372
(22) Application date: April 15, 1982

(72) Inventor: Yasunori SAKAGUCHI
Mitsubishi Electric Corp. Kitaitami Works, 1 Mizuhara 4-chome,
Itami City

(71) Applicant: Mitsubishi Electric Corp.
2-3 Marunouchi 2-chome, Chiyoda-ku, Tokyo

(74) Agent: Nobuichi KUZUNO, Patent Attorney, and 1 other party

Specification

1. Title of the Invention

Voltage gain control amplifier

2. Scope of the Patent Claims

(1) A voltage gain control amplifier characterized by being equipped with first and second transistors that perform differential amplification on signal input; third and fourth transistors that constitute a first differential circuit of the emitter junction in which the current distribution ratio varies depending on the gain control voltage and said emitter junction is connected to the collector of the aforementioned first transistor, and that supply the collector current of the aforementioned first transistor; fifth and sixth transistors that constitute a second differential circuit of the emitter junction in which the current distribution ratio varies depending on the gain control voltage and said emitter

junction is connected to the collector of the aforementioned second transistor, and that supply the collector current of the aforementioned second transistor; and a seventh transistor which constitutes the collector circuit of the aforementioned sixth transistor, of which the base is connected to a common collector resistor connected to both collectors of the aforementioned fourth and fifth transistors which similarly operate depending on the aforementioned gain control voltage, as well as to the collector to which both the aforementioned fourth and fifth transistors are connected, and of which the emitter is connected to the collector of the aforementioned sixth transistor via a collector resistor.

3. Detailed Explanation of the Invention

This invention pertains to a voltage gain control amplifier that changes gain depending on the magnitude of the applied DC voltage.

Figure 1 is a circuit diagram that shows an example of a conventional voltage gain control amplifier. (1) and (2) are npn transistors that constitute a differential pair, and (3) and (4) are first and second signal input terminals connected to the bases of transistors (1) and (2), respectively. The emitters of transistors (1) and (2) are connected to each other via resistors (5) and (6) which are connected in series, and a current source (7) is connected between the connection point and the ground point of resistor (5) and resistor (6). (8) and (9) are npn transistors that constitute a differential pair, and their emitters are both connected to the collector of transistor (1). (10) and (11) are npn transistors that constitute a differential pair, and their emitters are both connected to the collector of transistor (2). The collectors of transistors (8), (9) and (10) are all connected to a power supply terminal (12), and the collector of transistor (11) is connected to the power supply terminal (12) via a resistor (13). The bases of transistors (8) and (11) are both connected to a first control voltage terminal (14), and the bases of transistors (9) and (10) are both

connected to a second control voltage terminal (15). Also, an output terminal (16) comes out from the collector of transistor (11).

The operation of this conventional example is explained below. If the mutual conductance of the differential amplifier constructed of transistors (1) and (2) and resistors (5) and (6) and current source (7) is taken as g_{m1} , the DC voltage applied to the first control voltage terminal (14) is taken as V_1 , the DC voltage applied to the second control terminal (15) is taken as V_2 , and the resistance value of the resistor (13) is taken as R_L , then the gain of the voltage gain control amplifier shown in figure 1 exhibits the change as shown by the solid line in figure 2 depending on the value of $V_1 - V_2$. On the other hand, if the current of the current source (7) is taken as I_0 and the DC power supply voltage applied to the power supply terminal (12) is taken as V_{CC} , then the output DC potential at the output terminal (16) exhibits the change as shown by the dotted line in figure 2 depending on the value of $V_1 - V_2$.

Because the conventional voltage gain control amplifier is constructed as above, if the gain varies depending on the value of $V_1 - V_2$, then the output DC potential changes at the same time, and therefore it is difficult to connect it to the next amplification stage, and the amount of change of $V_1 - V_2$ accumulates in the output signal, and produces bad effects.

This invention was devised in order to eliminate the above drawbacks of conventional devices as described above, and its purpose is to provide a voltage gain control amplifier in which the output DC potential does not change in cases where the gain is varied depending on the control voltage $V_1 - V_2$.

Figure 3 is a circuit diagram that shows an implementation example of this invention. The same parts are shown by the same code numbers as in the conventional example of

figure 1, and their explanations are omitted. In this implementation example, a transistor (17) is inserted between the power supply terminal (12) and the resistor (13) in the collector circuit of the transistor (11). Its collector is connected to the power supply terminal (12), and its emitter is connected to the resistor (13). The collectors of transistors (9) and (10) are both connected, but they are not connected directly to the power supply terminal (12). Rather, they are connected to the power supply terminal (12) via a resistor (18), and this commonly connected collector is connected to the base of the transistor (17).

In the voltage gain control amplifier of this implementation example constructed as explained above, the change in gain in response to the value of $V_1 - V_2$ is completely the same as in the conventional example as shown by the solid line in figure 4. The change in output DC potential in response to the value of $V_1 - V_2$ is described below. If the DC bias voltages of the first signal input terminal (3) and the second signal input terminal (4) are equal, then the collector current of transistor (1) and the collector current of transistor (2) are equal, and they are both $I_0/2$. The collector current (I_{C8}) of transistor (8) and the collector current (I_{C9}) of transistor (9) vary depending on the value of $V_1 - V_2$, but if $I_{C8} = \alpha \times I_0/2$, then $I_{C9} = (1 - \alpha) \times I_0/2$ (where $0 \leq \alpha \leq 1$). Similarly, the collector current (I_{C10}) of transistor (10) and the collector current (I_{C11}) of transistor (11) are $I_{C10} = (1 - \alpha) \times I_0/2$, and $I_{C11} = \alpha \times I_0/2$. If the resistance of the resistor (18) is taken as R_L , then the base potential V_B of the transistor (17) is $V_B = V_{CC} - R_L (I_{C9} + I_{C10}) = V_{CC} - R_L (1 - \alpha) I_0$. Therefore, the output DC potential V_O at the output terminal (18) is

$$\begin{aligned} V_O &= V_B - V_{BE} - R_L I_{C11} \\ &= V_{CC} - R_L (1 - \alpha) I_0 - V_{BE} - R_L \alpha I_0/2 \\ &= V_{CC} - V_{BE} - \{ R_L (1 - \alpha) + R_L \alpha/2 \} I_0 \end{aligned}$$

$$= V_{CC} - V_{BE} - [R_L + \{(R_L/2) - R_1\} \alpha] I_0$$

Here, V_{BE} is the voltage between the base and the emitter of transistor (17). Therefore, if $R_L/2 = R_1$, then $V_O = V_{CC} - V_{BE} - R_1 I_0$, and there is no relationship to α . That is, the output DC potential V_O does not change depending on the control voltage. This is shown by the dotted line in figure 4.

Furthermore, if an AC signal voltage is applied between input terminals (3) and (4), the amount of change in the collector current I_{C9} of transistor (9) differs in phase from the amount of change in the collector current I_{C10} of transistor (10) by 180 degrees, and since its magnitude is equal, the sum current does not change, and it does not appear as a change of the base potential V_B of transistor (17), and therefore it also does not appear as a change to the output DC potential V_O .

Furthermore, in the above implementation example, a voltage gain control amplifier constructed of npn transistors is shown, but it can also be constructed of npn¹ transistors.

Also, in the above implementation example, the explanation is limited to DC voltage, but AC voltage can also be used, and in addition, if the output signal of this amplifier is controlled by a rectified current, it can become an automatic gain control (AGC) amplifier.

As stated above, by this invention, there is the effect that it can be easily connected to the next stage because a circuit that eliminates fluctuations in output DC potential depending on control voltage is added.

4. Brief Explanation of the Diagrams

Figure 1 is a circuit diagram that shows an example of a conventional voltage gain control amplifier; figure 2 is a characteristics diagram that shows the relationship

¹ This is a mistake in the original Japanese. It should probably say "pnp".

between gain control voltage and gain and output DC potential of this conventional example; figure 3 is a circuit diagram that shows an implementation example of this invention; figure 4 is a characteristics diagram that shows the relationship between gain control voltage and gain and output DC potential of this implementation example.

In the diagrams, (1) is a first transistor; (2) is a second transistor; (3) and (4) are signal input terminals; (8) is a third transistor; (9) is a fourth transistor; (10) is a fifth transistor; (11) is a sixth transistor; (13) is a collector resistor; (14) and (15) are gain control voltage terminals; (17) is a seventh transistor; (18) is a common collector resistor.

Furthermore, in the diagrams, the same code numbers represent the same or equivalent parts.

Agent: Nobuichi KUZUNO, and one other party

Key to the figures

Figure 2

[Left axis] Gain
[Top center, dotted line] Output DC potential
[Right axis] Output DC potential
[Center, solid line] Gain

Figure 4

[Left axis] Gain
[Left center, dotted line] Output DC potential
[Right axis] Output DC potential
[Right center, solid line] Gain